Amendments to the Abstract

On page 8, please amend the Abstract as follows:

An improved segmented digital to analog converter is provided, configured with a novel method of compensating current flow in secondary or successive segmented elements. In operation, dual current devices initially load, then subsequently unload a cascade of resistor networks connected to the secondary or successive voltage segmenting elements, preventing the perturbation of precise operation of the primary or preceding elements. In contrast to conventional approaches, the improved converter obviates the need for a buffer or amplifier to isolate the secondary and successive voltage segmenting elements from the primary or preceding elements. In further contrast to conventional devices, a second and third successive voltage segmenting elements, where a third segmented series of resistors has a third set of resistors connected end to end from along which an output can be generated at any point between the resistors, wherein the third segmented series of resistors further includes one current source connected at one end of the third series of resistors, and a second current source connected at another end of the third series of resistors.

Amendments to the claims:

Claims 1-4: Please Cancel Claims 1-4

5. (Currently Amended) A segmented digital to analog converter, comprising:

a first segment having a first plurality of resistors and configured to receive and convert one set of digital bits of a digital input signal to an analog signal;

a second segment configured to receive and convert a second set of digital bits of the input signal to an analog signal, the second segment having a second series of resistors configured to receive the first set of digital bits, a first current source connected at one end of the second series of resistors, and a second current source connected at another end of the second series of resistors; and

a third segment having a third segmented series of resistors including a third set of resistors connected end to end from along which an output can be generated at any point between the resistors;